What is claimed is:

1 A method for the application of a gating signal in a double gate FET, which comprises applying, in response to a first signal fed into a first gate electrode, a second signal that has a same signal-level temporal-change direction as the first signal and has a signal level shifted by a predetermined magnitude to a second gate electrode.

2. A method for the application of a gating signal in a double gate FET, which comprises applying, in response to a first signal fed into a first gate electrode, a second signal that has a same signal-level temporal-change direction as the first signal and has a slower or faster rise time or a fall time to a second gate electrode.

3. A method for the application of a gating signal in a double gate FET, which comprises applying, in response to a first signal fed into a first gate electrode, a second signal that has a same signal-level temporal-change direction as the first signal and has a predetermined time difference to a second gate electrode.

4. An integrating circuit furnished with a double gate FET utilizing the method for the application of a gating signal set forth in any one of claims 1 to 3.